MEMORY DEVICES HAVING BIT LINE PRECHARGE CIRCUITS WITH OFF CURRENT PRECHARGE CONTROL AND ASSOCIATED BIT LINE PRECHARGE METHODS

Abstract of the Disclosure

A memory device having an off-current (Ioff) robust precharge control circuit and a bit line precharge method are provided. The precharge control circuit may be embodied as a delay circuit unit which receives and delays a precharge enable signal for a predetermined delay time; a NAND gate which receives the precharge enable signal and the output of the delay circuit; and an inverter which inverts the output of the NAND gate. The precharge control circuit may enable the word lines before disabling the precharge signal.